DESIGN AND ANALYSIS OF FIVE-INPUT MULTIPLE-FUNCTIONQCA AMONG THE ALTERNATIVE TECHNOLOGIES

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ABSTRACT

Quantum-dot Cellular Automata (QCA) are among the alternative technologies that enable nanoscale circuitdesign of high performance and low power consumption features. This work showcases an extensive structuraland power analysis of previous 5-input majority gates. We found that the existing 5-input majority gates are notpower efficient, and the structures are not well optimized. To overcome this, we proposed a new low-complexitycoplanar 5-input majority gate, which consumes less power compared to prior designs. A novel 1-bit full addercircuit is presented to evaluate the suitability of the proposed gate. The Majority Gates forms the basic building blocks in QCA circuit design. The Three-input Majority Gate is widely used in the design and synthesis of the circuits. The Clock cycle which controls the flow of data cannot be reduced and hence the hardware complexity of the circuit is reduced by focusing on increasing the number of Inputs to the Majority gate. In this paper, a novel nine-input Majority Gate and eleven input majority gate has been proposed which reduces the cell count and offers good scalability. Also,the proposed gate is a feasible solution for the recently proposedUSE (Universal, Scalar and Efficient) clocking scheme. In orderto demonstrate the flexibility and area efficiency of our 5-inputmajority gates we implement two designs: a full adder and aRAM cell block. These designs have been implemented using afree and a regular (USE) clock schemes. Our results show areareductions up to 50% compared to state-of-the-art designs.

1. INTRODUCTION

The push to scale the conventional MOSFET continues to show remarkable progress in Semiconductor industry. There are indications that in recent years, this scaling down has slowed down due to quantum-mechanical tunnelling of carriers through the thin gate oxide and from source to drain [1]. Many other things such as interconnects and metals should also be scaled with respect to the transistor scaling. Also packing more transistors in a small area is leading to huge power consumption and heat dissipation during the switching cycle. Because of these interconnect problem and power dissipation problem, it is anticipated that VLSI Industry is searching for an innovative device to overcome these problems. One such devices was Quantum dot Cellular Automata (QCA), proposed by Lent et al in 1993.

A QCA cell is basically a nanometric square with fourquantum dots and two electrons that can perform tunnelling between the dots [1]. Due to Couloumb interactions, thereare only two stable configurations of the electrons inside thecell, as shown in Fig. 1. The black dots are the quantum dotscontaining an electron. Polarizations P = -1 and P = +1represent logic states 0 and 1, respectively. Bistable cellsare locally connected through field effect forces and can beorganized in such a way that computation is performed.

With the exponential decrease in feature size in CMOS technology,devices are more prone to high leakage current, high power density,and are more sensitive to thermal noise [1]. These deficiencies encourageresearchers to explore alternative technologies like QuantumdotCellular Automata (QCA), Tunneling Phase Logic (TPL), SingleElectron Tunneling (SET), and Carbon nanotube (CNT). QCA could be afeasible alternative that has none of the above problems and promisesoperation at high frequency with low power consumption and highdevice density [2–4]. QCA is based on the confinement and mutualrepulsion of electrons. The fundamental element in QCA is a squaredcell with four dots and two excess electrons. Therefore, unlike theconventional CMOS, a change in logic value from 1 to 0 does not yielddischarging of the capacitor. It also offers a new horizon in informationcomputation. The information is

transferred as a result of the propagationof polarization between two cells, due to the Coulombic interactionof electrons. There is no flow of current as in conventionalCMOS. Hence, power dissipation due to change in logic value andpropagation does not add up to the total power dissipation [5]. Thisfeature makes QCA useful for computation.

Different QCA based digital circuits have investigated during recentyears; structures for 5-input majority gate, designs for a 1-bitfull adder, QCA based memory cells, flip-flopsalso have been studied. The idea behind this work is to devisepower efficient QCA circuits and analyze the power dissipation of existingand proposed 5-input majority gates. The proposed 5-input majoritygate requires fewer cells and draws lower power compared to thebest-reported one in the literature. Further, an optimal single layer 1-bitfull adder is designed by considering the proposed gate.

QCA Cell Model

1.1 Isolated QCA Cell

A QCA contains four quantum dots aligned in a square area separated by a distance, sufficient enough for the electrons to tunnel from one dot to another (shown in Fig1).

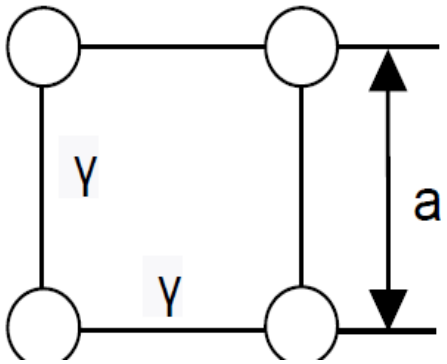

Figure1. Image of QCA Cell

1.2 Cell - Cell coupling

The electrons tunnel only through Quantum dots within the cell. They do not tunnel between the Quantum dots of adjacent cells. Polarity of a QCA Cell is influenced by the polarity of the nearby cells. The abruptness of cell-cell response function depends on the ratio of strength of tunneling energy to coulomb energy of electrons on neighbouring cells. By fixing the polarization of cell 1, the coulombic effect on the polarization of cell2 is measured. By changing the polarization of cell 1 from -1 to +1 the coulombic effect of it on polarization of cell2 is observed and shown in the Fig2.This nonlinearity and bistable saturation of this response is same as gain of a conventional buffer in a CMOS technology.

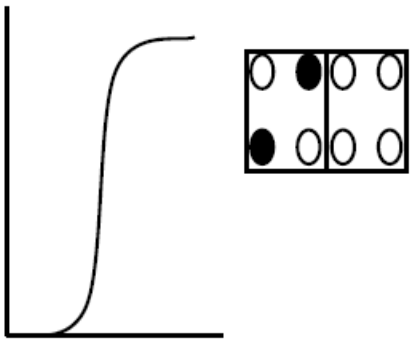

Figure 2. Cell Polarities Image

2. LITERATURE REVIEW

Quantum-Dot Cellular Automata is an alternative to current CMOS technology which encounters leakage and short channel effects when further Scaling is done. The Majority Gates forms the basic building blocks in QCA circuit design. The Three-input Majority Gate is widely used in the design and synthesis of the circuits. The Clock cycle which controls the flow of data cannot be reduced and hence the hardware complexity of the circuit is reduced by focusing on increasing the number of Inputs to the Majority gate. In this paper, a novel nine-input Majority Gate and eleven input majority gate has been proposed which reduces the cell count and offers good scalability.

QCA (Quantum-dot Cellular Automata) is a promisingnew technology with low power consumption and high speedthat allows the design of nanoscale integrated circuits. The 3-input/1-output majority gate is the basic building block in QCAcircuits. This work presents a new design of a multi-output, 5-input majority gate. Our proposed gate is quite useful because itsoutputs can present different configurations with several logicalfunctions at once, enabling the design of smaller circuits. Also,the proposed gate is a feasible solution for the recently proposedUSE (Universal, Scalar and Efficient) clocking scheme. In orderto demonstrate the flexibility and area efficiency of our 5-inputmajority gates we implement two designs: a full adder and aRAM cell block. These designs have been implemented using afree and a regular (USE) clock schemes. Our results show areareductions up to 50% compared to state-of-the-art designs.

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design of high performance and low power consumption features. This work showcases an extensive structuraland power analysis of previous 5-input majority gates. We found that the existing 5-input majority gates are notpower efficient, and the structures are not well optimized. To overcome this, we proposed a new low-complexitycoplanar 5-input majority gate, which consumes less power compared to prior designs. A novel 1-bit full addercircuit is presented to evaluate the suitability of the proposed gate.
The results demonstrate that the proposedfull adder performs equally well compared to existing multilayer designs, and performs better in the case ofprevious coplanar full adder designs in all aspects. Our design achieves 22% reduction in cell count and takes18% less area in comparison to the best single layer design. Furthermore, it produces an equal delay, whencompared to the best design in this segment. The QCADesigner tool is used to validate the layout of the proposeddesigns and the QCAPro power estimator tool is used to evaluate the power dissipation of all considered designs.Our results clearly demonstrate that, the hardware requirement for a QCA design is reduced and circuits becomesimpler in level, gate counts and clock phases by considering proposed gate.

3. EXISTING MAJORITY GATES

The already existing majority gates in the literature are the Three-input (as shown in Fig.3), the Five-input, the Seven-input majority gate and the nine input majority gate. The Five-input, Seven-input gates and nine input majority gates are discussed in this section now.

3.1 Five Input Majority Gate

The five input majority gate discussed in [24] is a co planar structure with a reduced cell count and latency. The Majority Gate Function of the Five Input Majority Gate is given by,

$$M(A, B, C, D, E) = F = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE$$

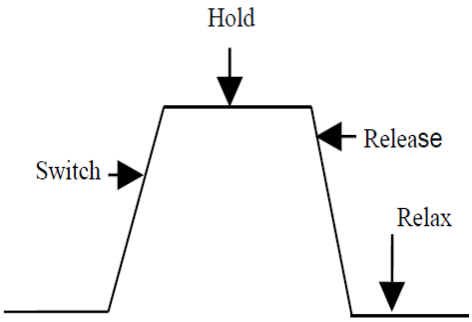

Figure 3: CLOCKING Image

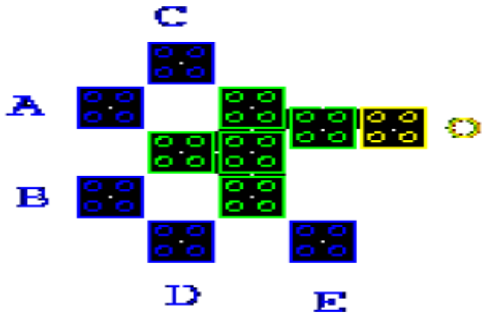

Figure 4: Five Input Majority Gate

The Five input majority voter simulation for the logic function given by the equation no above is given in the Fig 4. The Majority Voter can be implemented as AND and OR gates using -1 and +1 Polarisations,

$$M(A, B, C, 0, 0) = F = A.B.C + A.B.0 + A.B.0 + A.C.0 + A.C.0 + A.0.0 + B.C.0 + B.C.0 + B.0.0 + C.0.0 = A.B.C$$

The Seven Input Majority Gate

The Design proposed in the work of [16], makes use of Seven Input cells and Drive cells with Co Planar Crossing. With a high input

gate we can reduce the cell count and the circuit size in complex multi-bit QCA circuitry and increases the effective utilization of substrate space. The equations are

$$M(A, B, C, D, 0, 0, 0) = A.B.C.D$$

$$M(A, B, C, D, 1, 1, 1) = A + B + C + D$$

4. PROPOSED METHODOLOGY

In this section, we present the designs of a full adder and aRAM memory cell to demonstrate the area reduction achievedby the adoption of our MAJ5 gate in QCA circuit designs.For both designs we have implemented the free and the regular(USE) clock schemes layouts.

A. Full adder

Fig. 5 shows the QCA adder majority gate-level representation.Our adder uses two MAJ5 gates to simplify the designlayout. Traditional designs use three 3-input majority gates(MAJ3), wires, and inverters. Moreover, our design takesadvantage of the MAJ5 ability to implement a multiple-outputMAJ3, by fixing the values of inputs D and E in +1 and -1,respectively. We need two results from one gate at the sametime, one is a 3-input majority function to calculate the carryand the other is a 3-input minority as inputs to calculate thesum. The full adder is shown in Fig. 6.

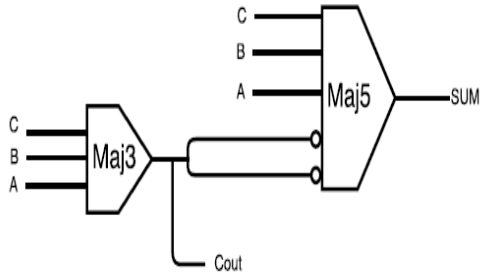

Fig. 5. Full adder schematic.

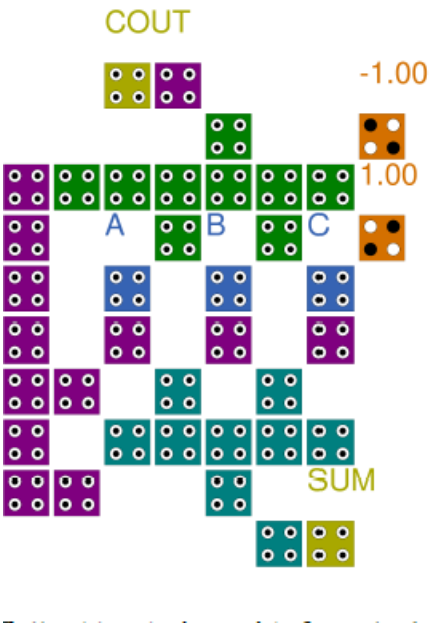

Fig. 6. Full adder design with free clock scheme.

In order to demonstrate that our design is suitable to USE,we build another adder with this clock scheme. The adderimplemented with USE clock scheme is shown in Fig. 7. Here,we have applied the multilayer approach to implement wirecrossing. We have used the same schematic presented in Fig. 5,but considering all USE restrictions.

B. RAM memory cell

Another interesting circuit that takes advantage of ourproposed MAJ5 is the RAM memory cell [5]. Fig. 8 reveals the schematic of the circuit, having three MAJ3 and oneMAJ5 gates. The leftmost MAJ3 implements an AND gateand its outputs are connected as inputs in the other two MAJ3.The latter are simple 2-input AND gates with a single output.Finally, they connect to a MAJ5.Fig. 9 shows our proposed design of the RAM memory cellcircuit in QCA, considering a free clock scheme. The leftmost

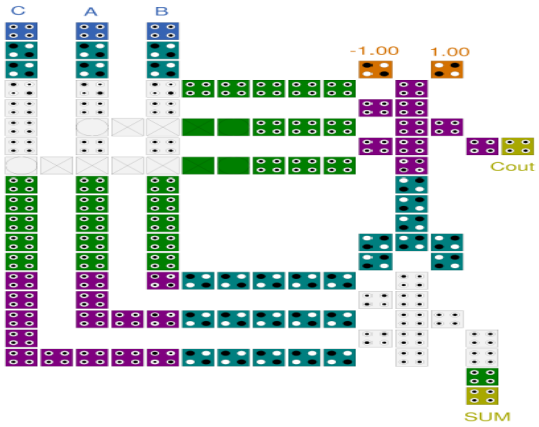

Fig. 7. Full adder design with USE clock scheme.

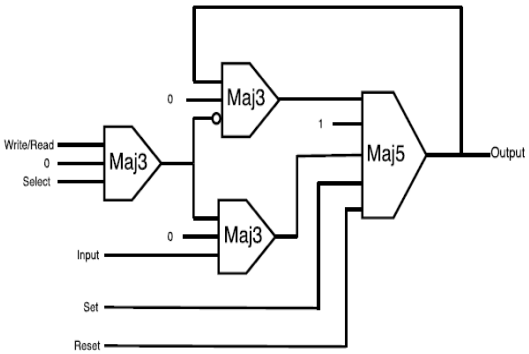

Fig. 8. Schematic of RAM cell proposed in [5].

MAJ3 of Fig. 8 is implemented by a MAJ5 in order toexploit its multiple outputs features. The other two MAJ3

are implemented using traditional majority gates. Finally, the MAJ5 receives its inputs and provides the result, alsoexploiting the multiple outputs, since the result of the RAMcell is an input in the uppermost MAJ3 of Fig. 6.

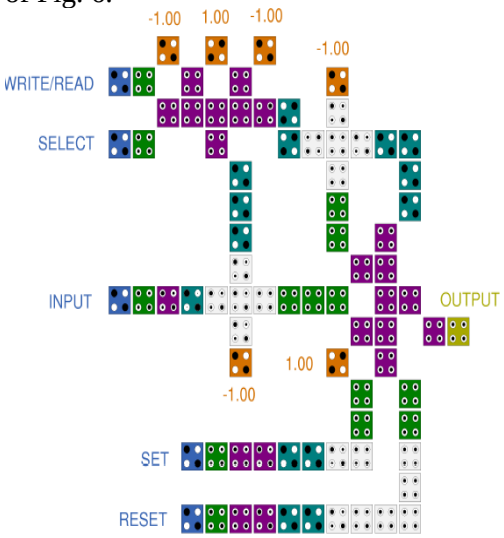

Fig. 9. RAM memory implemented with free clock scheme.

We also follow the schematic of Fig. 6 to implement theRAM memory cell using the USE clock scheme. Again, weapply one MAJ5 to implement a 2-input AND gate withmultiple outputs and a MAJ5 in the output of the circuit.The two normal majority gates have diagonal inputs in order torespect the restrictions of USE cells, as proposed in [4].

CONCLUSION

In this work, we proposed a novel 5-input, multi-output majoritygate for QCA technology. Our gate has several featuressuch as: two outputs that can be configured as both majorityor minority; ability to perform different logic functions bysimple fixing some of the inputs; efficient layout in free andUSE clock schemes. We used our gate to implement a fulladder and a RAM memory cell designs. For both designs wehave implemented free and USE clock schemes. QCAPro, a power estimation tool was used to investigate leakage powerand switching power dissipation, and all designs were realized andevaluated using QCADesigner 2.0.3 tool. Further, to showcase the efficacyof the proposed majority gate, a new 1-bit full adder structure circuits with respect to existing coplanar designs. The results confirmedthat the presented structures have outperformed all prior designs interms of the new cost function and showed significant improvements interms of complexity, area occupation and input to output clock delay ascompared to most of the coplanar designs. The proposed optimalstructures can lead to designing of more complex and high-performanceQCA nanoscale circuits in the future.

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